MM23SC4452
256Byte EEPROM with write/read protect function and PSC

27 September 2006

256 BYTE EEPROM
With Write Protect and Read Protect Function and Programmable Security Code (PSC)

Features

- Standard CMOS process
- 256 x 8 bits EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 0..31)
- 3-byte Programmable Security Code (PSC) for memory write/ erase protection
- Single 5V power supply for read and write/ erase
- Low power operation: 3mA typical active current
- 2.5ms programming time
- 2-wire serial interface
- End of processing indication
- ISO standard 7816 compatible
- High reliability:
  - 1,000,000 erase/ write cycles guaranteed
  - 10 years data retention
- Wide operating temperature range, 0 to 70°C
- MM23SC4452 “Enhanced” version enables additional read protection.

Description

MM23SC4452 contains 256 x 8 bits of EEPROM main memory and a 32 x 1 bit protection PROM memory. Random read access to any byte in the memory is not possible except to certain areas of the memory.

During memory erase, all 8 bits of a byte are set to logical one. During memory write, individual bit(s) are set to logical zeros depend on the data value to be written. Normally, a data change may consist of an erase and then write operation. The write or erase operation takes at least 2.5ms to complete.

The first 32 bytes (Address: 0 to 31) in memory are irreversibly protected by the corresponding 32 protect bits in the 32 x 1 bit protection memory. The 32 protect bits are one-time programmable and cannot be erased once they are set to logical zero.

MM23SC4452 also provides a 3-bit Error Counter (EC) and three bytes Programmable Security Code (PSC) to prevent unauthorized erase/ write operation to the memory.

The entire memory array except the first 20 bytes addresses (00H-13H) is unreadable upon power on reset. Refer to Figure 1c. The memory can be fully read, written or erased only after PSC verification. If the user fails to enter the correct PSC in three consecutive attempts, the device will block any further PSC entry attempts and the memory can never be read, erased or written again.

The PSC bytes are pre-programmed by the manufacturer with a code, which is specified for device transport security purposes, before the device are shipped to the customer. The Error Counter will be pre-erased by the manufacturer to allow maximum attempts for PSC entry.

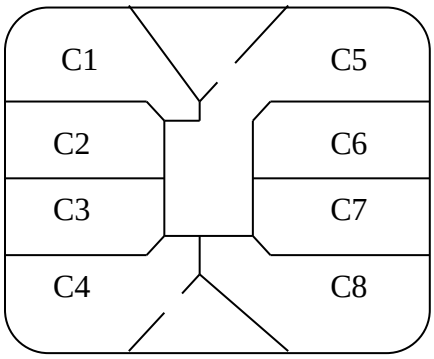


Figure 1a: Pin Configuration for M2

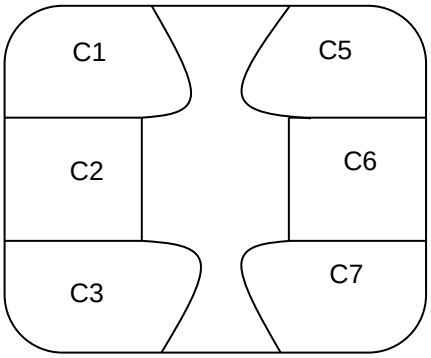


Figure 1b: Pin Configuration for M3

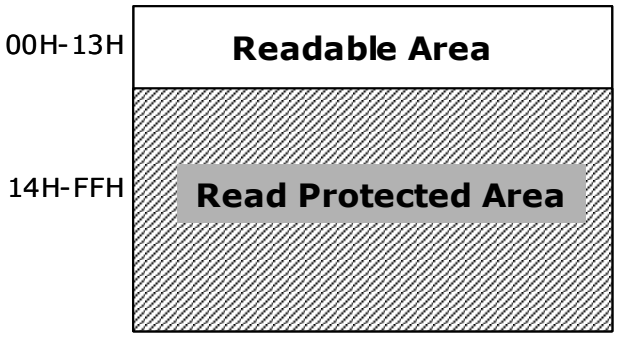


Figure 1c: Read Protection Area for Enhanced MM23SC4452

Definitions and Functions

Card Contact (M2)	Symbol	Description
C1	VCC	Supply Voltage
C2	RST	Reset
C3	CLK	Clock Input
C4	NC	No Connect
C5	GND	Ground
C6	NC	No Connect
C7	I/O	Bidirectional Data I/O (Open drain)
C8	NC	No Connect

Note: An external pull up resistor is needed to be connected to the I/O pin.

Memory Overview

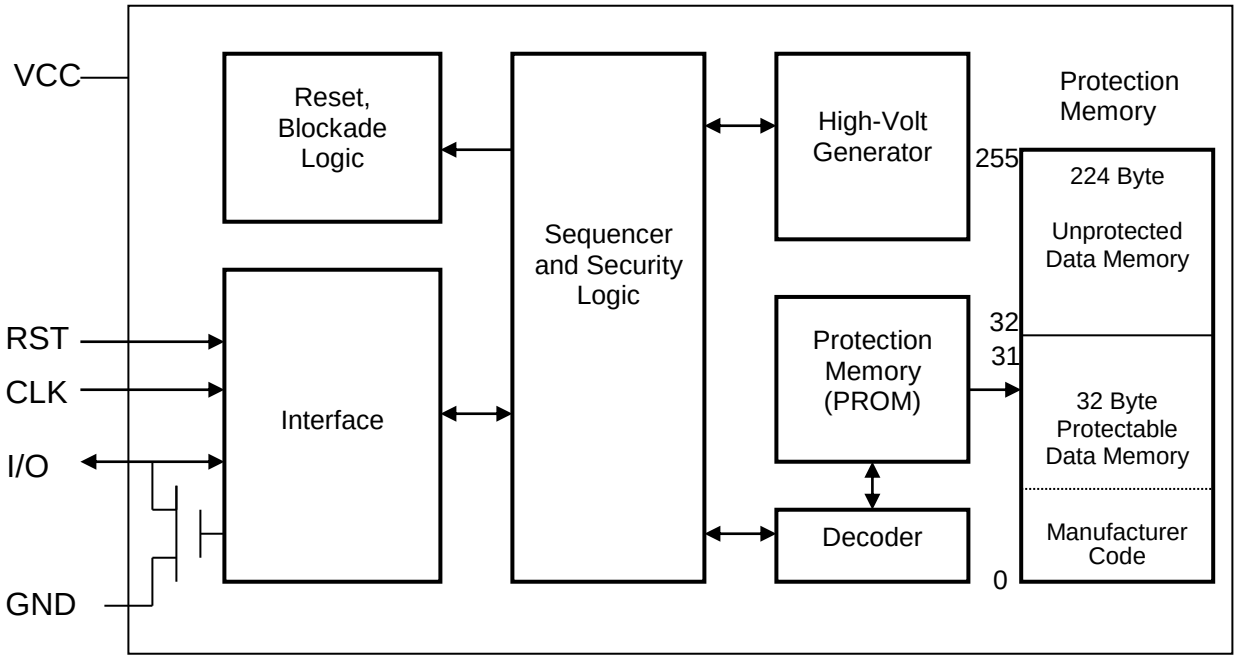


Figure 2: Memory Overview

Functional Description

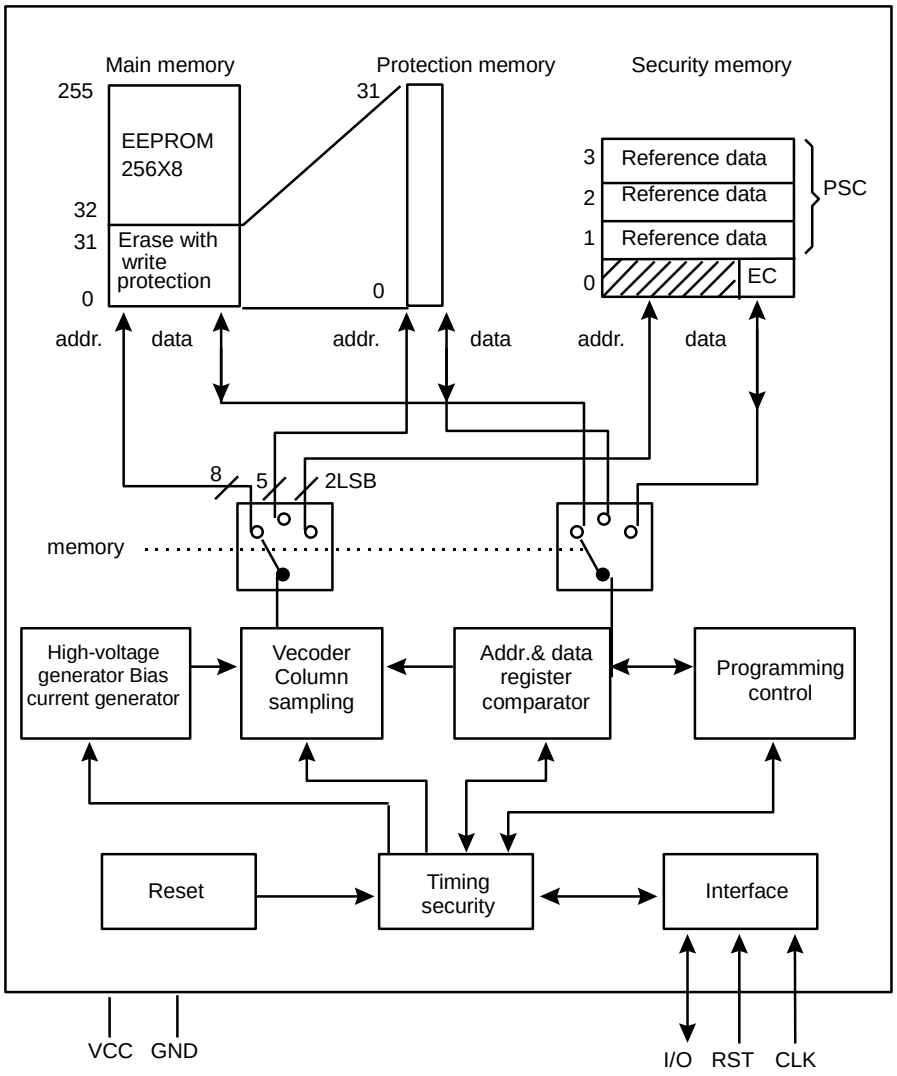
The MM23SC4452 works on a 2-wire serial transmission protocol. Data is input or output from the chip through the I/O pin at the falling edge of CLK. There are four modes of operations:

Reset and Answer-to-Reset
Command Mode
Outgoing Data Mode
Processing Mode

Reset and Answer-to-Reset

The Answer-to-Reset operation confirms to ISO 7816-3 ATR standard. The reset action can be invoked at any time during operation to terminate any active command operation. With RST keeps High, the internal address counter is set to zero by the CLK pulse. The LSB of the first byte data in the memory will be output from I/O when RST goes from High to Low. By continuing to send pluses to CLK, the contents of the first four bytes will be output from I/O pin. After the ATR process completes, the I/O pin will be set to high impedance.

Block Diagram



Functional Description

The MM23SC4452 contains 256 bytes EEPROM main memory (see block diagram) and 32 bits protection memory. The main memory is byte-wise erased and written. When the memory is erased, 8 bits of a data byte are all set to logic 1. When the memory is written, a data byte can be programmed bit by bit set to logic 0 according to the logic and between the old and the new data. Generally, updating a data includes an erase and a write procedure. When updated, new input data and the contents of the old data are compared so that if none of the 8 bits requires a logic 0 to 1 change the erase operation will be skipped. On the contrary, the write operation will be skipped if no logic 1 to 0 change is necessary. Write and erase operation takes at least 2.5ms each.

The first 32 bytes can be protected individually by writing the corresponding bit in the protection memory. Each data byte in the address range and its assigned bit in the protection memory have the same address. Once the protection bit written it cannot be erased.

The security memory of MM23SC4452 contains an error counter (bit0-bit2) and 3 bytes reference data. The three bytes reference data are as a whole called programmable security code (PSC). Upon power on, the MM23SC4438 would not allow any read access except to the address from 00H to 13H, including ATR. Read access to the whole main and protection memories are only enabled when correct PSC is entered. In the security memory area, except for the error counter value, the content of the PSC addresses (01H, 02H and 03H) cannot be read out.

The error counter can always be written. After three successive unsuccessful PSC verification, the error counter will block the chip, any write and erase operation to the memory will be forbidden.

Transmission Protocol

Transmission Mode

The transmission protocol is a two-wire link protocol between the interface device IFD and IC. The protocol type is “S=10”. All data changes on I/O are triggered by the falling edge on CLK.

The transmission protocol is composed of the 4 modes:

- Reset and answer-to-reset
- Command mode
- Data output mode
- Processing mode

Reset and Answer-To-Reset

Answer-To-Reset takes place according to ISO7816-3. During operation, the reset can be given at any time. During reset, the address counter is set to zero; when RST is set from high level to low level, the lowest bit of the first byte is read out on I/O. Under continuous 31 clock pulses the contents of the first 4 bytes EEPROM addresses can be read out. The 33rd clock pulse set I/O to high impedance. During Answer-To-Reset, any start and stop condition is ignored.

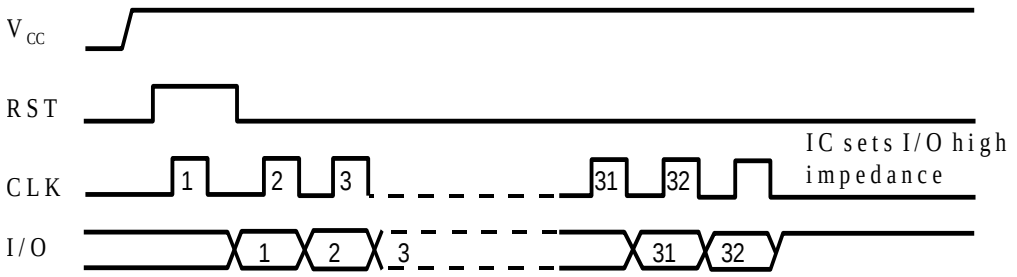


Figure 3: Reset and Answer-To-Reset

Command Mode

After Answer-To-Reset, MM23SC4452 waits for a command entry. Each command begins with a start condition, includes three bytes command entry and ends of a stop condition.

- Start condition: during CLK in high level, a falling edge on I/O
- Stop condition: during CLK in high level, a rising edge on I/O

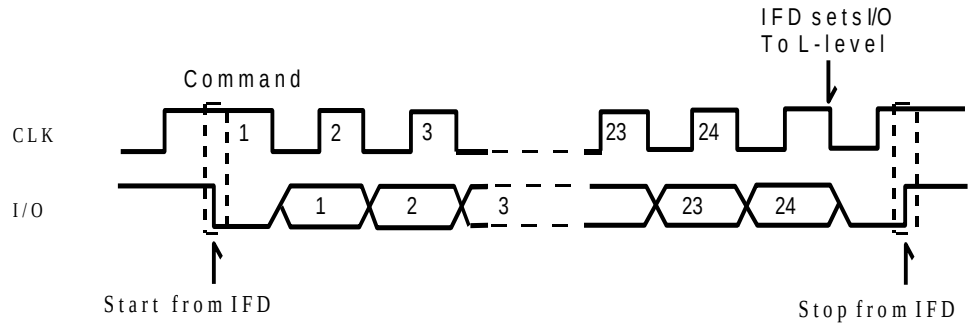


Figure 4: Command Mode

- After receiving a command, there are two possible modes:
- Data output mode for reading
- Processing mode for writing and erasing

Data Output Mode

In reading, the chip sends the data to IFD. Figure 5 shows the timing diagram. After the first falling edge on CLK, the first bit on I/O is valid. After the last data bit, an additional CLK pulse is necessary in order to set I/O to high level for receiving a new command. During this mode any start and stop condition is ignored.

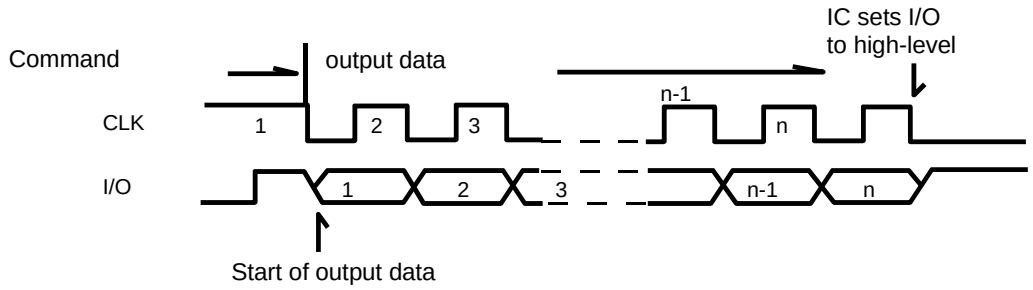


Figure 5: Data Output Mode

Processing Mode

During processing, the chip processes internally. Figure 6 shows the timing diagram. The IFD has to send clock to the chip continuously until I/O is set to high level which has been set to low level on the first falling edge of CLK. During this mode any start and stop condition is ignored.

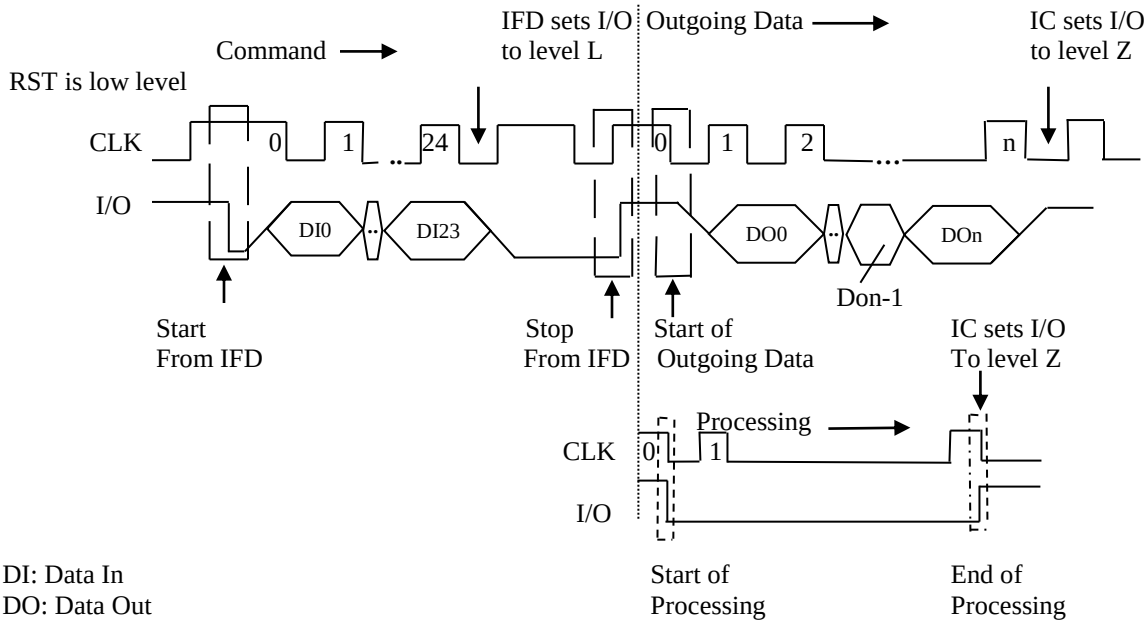


Figure 6: Processing Mode

Commands

Command Format

MM23SC4452 provide seven commands that are listed in Table1. Every command consists of three bytes.

MSB Control LSB	MSB Address LSB	MSB Data LSB
B7 B6 B5 B4 B3 B2 B1 B0	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0

Command transmission begins with the control byte LSB.

Table 1

Control of Byte 1								Address of Byte2	Data of Byte3	Operation	Mode
B7	B6	B5	B4	B3	B2	B1	B0	A7~A0	D7~D0		
0	0	1	1	0	0	0	0	Address		Read Main Memory	Data Output
0	0	1	1	1	0	0	0	Address	Input Data	Update Main Memory	Processing
0	0	1	1	0	1	0	0			Read Protection Memory	Output Data
0	0	1	1	1	1	0	0	Address	Input data	Write Protection Memory	Processing
0	0	1	1	0	0	0	1			Read Main Memory	Data Output
0	0	1	1	1	0	0	1	Address	Input Data	Update Main Memory	Processing
0	0	1	1	0	0	1	1	Address	Input Data	Compare Data	Processing

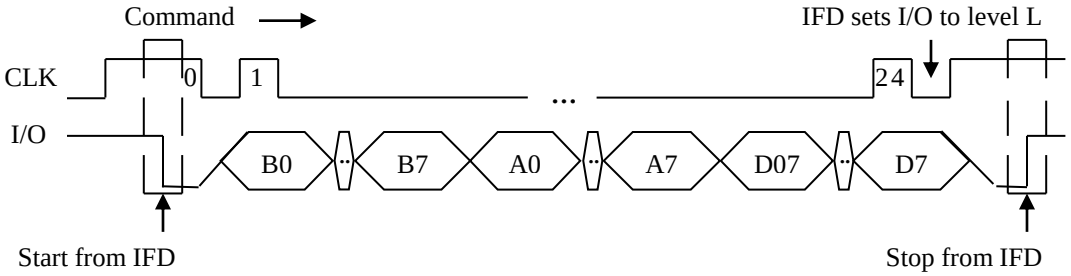


Figure 7: Command Mode

Command Description

Read Main Memory

The command reads out the memory contents from the given address (N) to the last address of the memory (with LSB first). After the command entry, the IFD has to provide sufficient clock pulses. The number of the clock pulse = (256-N)x8+1.The main memory can always be read.

Address (decimal)	***Main Memory***	***Protection Memory***	***Security Memory***
255	Data Byte 255 (D7…D0)	-	-
:	:	-	-
32	Data Byte 32 (D7…D0)	-	-
31	Data Byte 31 (D7…D0)	Protection Bit 31 (D31)	-
:	:	:	-
1	Data Byte 1 (D7…D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7…D0)
0	Data Byte 0 (D7…D0)	Protection Bit 0 (D0)	Error Counter

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	0	0	Address	No Effect
Hexadecimal	30_H								00_H…FF_H	No Effect

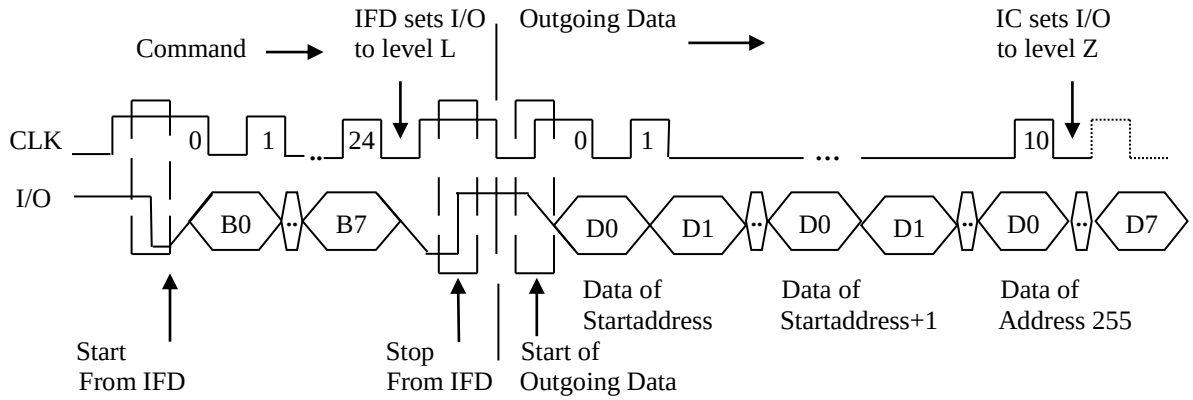


Figure 8: Read Main Memory

Read Protection Memory

The command reads out 32 bits to I/O on continuous 32 clock pulses. By an additional clock pulse the I/O is set to high level. The protection memory can always be read.

Address (decimal)	***Main Memory***	***Protection Memory***	***Security Memory***
255	Data Byte 255 (D7…D0)	-	-
:	:	-	-
32	Data Byte 32 (D7…D0)	-	-
31	Data Byte 31 (D7…D0)	Protection Bit 31 (D31)	-
:	:	:	-
1	Data Byte 1 (D7…D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7…D0)
0	Data Byte 0 (D7…D0)	Protection Bit 0 (D0)	Error Counter

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	1	0	0	No Effect	No Effect
Hexadecimal	34_H								No Effect	No Effect

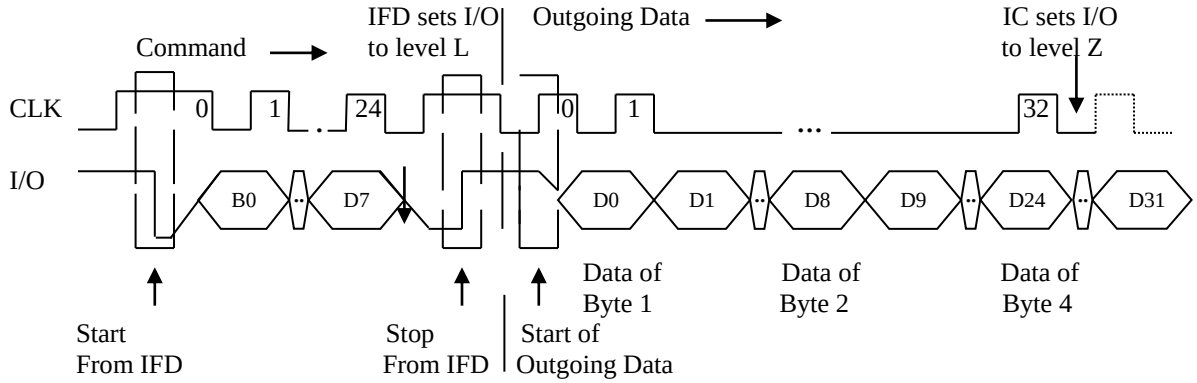


Figure 9: Read Protection Memory

Read Security Memory

The three bytes reference data can only be read after successful PSC verification, otherwise the output of the PSC will be suppressed and I/O is set to low level. The error counter can always be read. Read out 4 bytes security memory requires 32 clock pulses, I/O is set to high level by an additional pulse.

Address (decimal)	***Main Memory***	***Protection Memory***	***Security Memory***
255	Data Byte 255 (D7…D0)	-	-
:	:	-	-
32	Data Byte 32 (D7…D0)	-	-
31	Data Byte 31 (D7…D0)	Protection Bit 31 (D31)	-
:	:	:	-
1	Data Byte 1 (D7…D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7…D0)
0	Data Byte 0 (D7…D0)	Protection Bit 0 (D0)	Error Counter (0,0,0,0,0,D2,D1,D0)

	Control								**Address**	**Data**
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	0	1	No Effect	No Effect
Hexadecimal	31_H								No Effect	No Effect

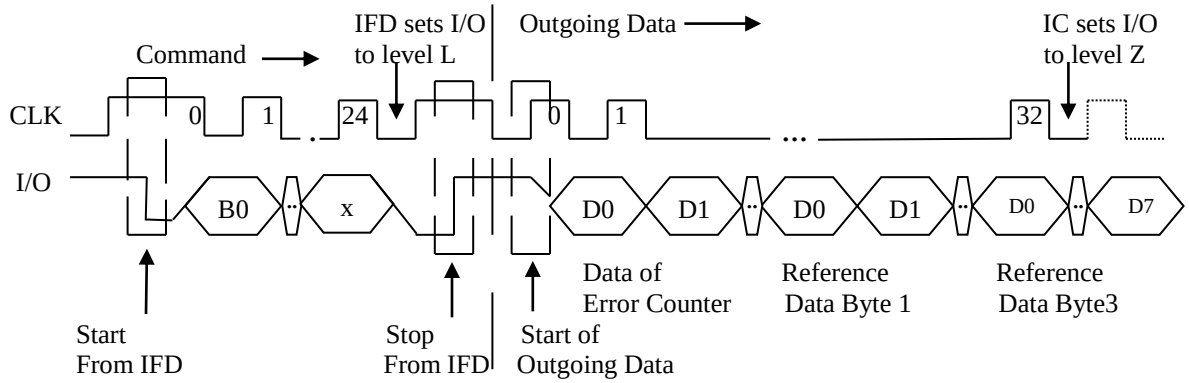


Figure 10: Read Security Memory

Update Main Memory

The command programs the addressed EEPROM byte with the given data byte. Depending on the old and the new data, one of the following operations will take place during processing mode.

- Erase and write (5ms) corresponding to m=255 clock pulses
- Write only (2.5ms) corresponding to m=124 clock pulses
- Erase only (2.5ms) corresponding to m=124 clock pulses
  (Frequency of clock=50 kHz)

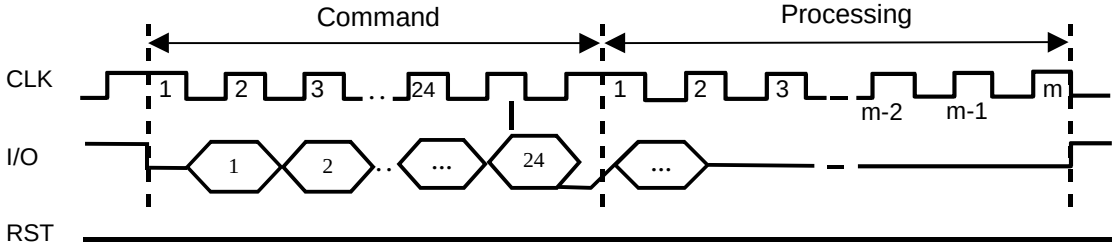


Figure 11: Update Main Memory

Address (decimal)	***Main Memory***	***Protection Memory***	***Security Memory***
255	Data Byte 255 (D7…D0)	-	-
:	:	-	-
32	Data Byte 32 (D7…D0)	-	-
31	Data Byte 31 (D7…D0)	Protection Bit 31 (D31)	-
:	:	:	-
1	Data Byte 1 (D7…D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7…D0)
0	Data Byte 0 (D7…D0)	Protection Bit 0 (D0)	Error Counter

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	0	0	0	Address	Input Data
Hexadecimal	38_H								00_H…FF_H	Input Data

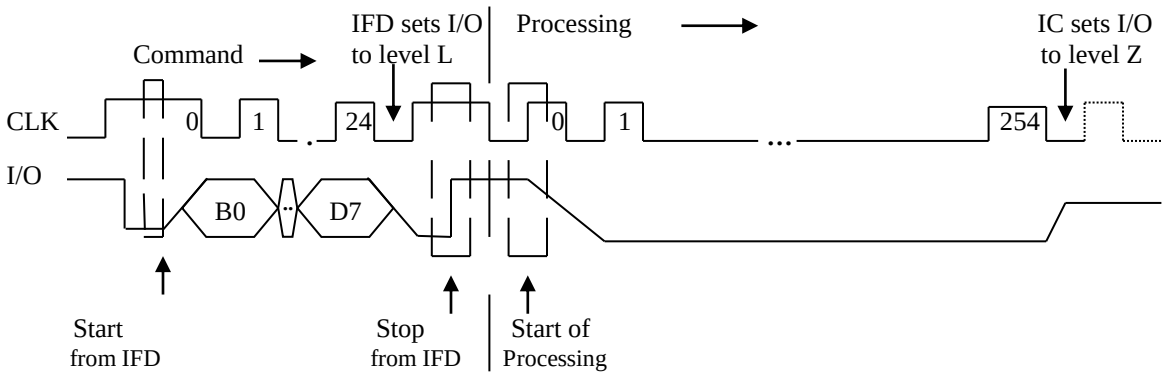


Figure 12: Erase or Write Main Memory

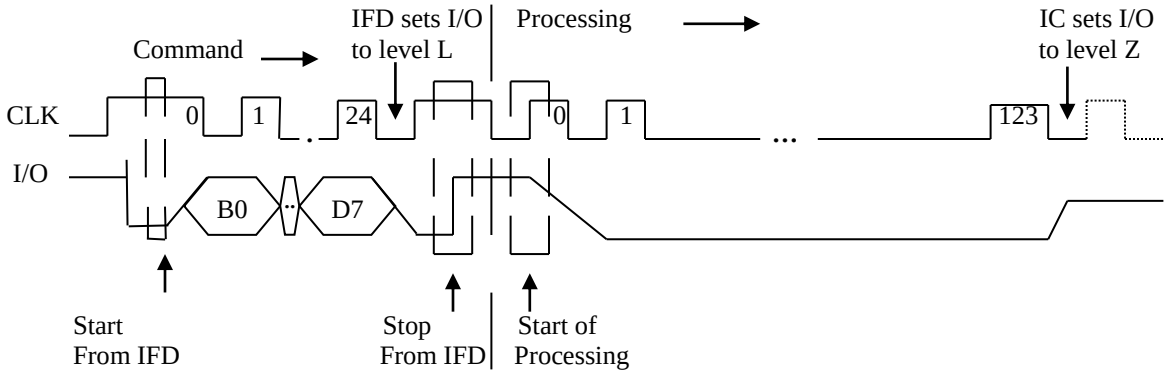


Figure 13: Erase or Write Main Memory

Update Security Memory

After successful PSC verification, the reference data can be updated. Otherwise only the error counter can be written. The processing time and the required clock pulses are the same as that of update main memory.

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	0	0	1	Address	Input Data
Hexadecimal	39_H								00_H…03_H	Input Data

Write Protection Memory

The execution of this command includes a comparison of the given data byte and the assigned byte in the main memory. If the result is data identity, the protection bit is written so that the corresponding data byte in the main memory is unchangeable. If the result is differences, the protection bit cannot be written. The execution time and clock pulses are the same as that of update main memory.

Address (decimal)	***Main Memory***	***Protection Memory***	***Security Memory***
255	Data Byte 255 (D7…D0)	-	-
:	:	-	-
32	Data Byte 32 (D7…D0)	-	-
31	Data Byte 31 (D7…D0)	Protection Bit 31 (D31)	-
:	:	:	-
1	Data Byte 1 (D7…D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7…D0)
0	Data Byte 0 (D7…D0)	Protection Bit 0 (D0)	Error Counter

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	1	1	0	0	Address	Input Data
Hexadecimal	$3C_H$								00_H…$1F_H$	Input Data

Compare Verification Data

Only after the error counter has one bit written procedure, compare verification data can be executed. The command compares the given verification data byte with the corresponding reference data byte.

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7…A0	D7…D0
Binary	0	0	1	1	0	0	1	1	Address	Input Data
Hexadecimal	33_H								00_H…03_H	Input Data

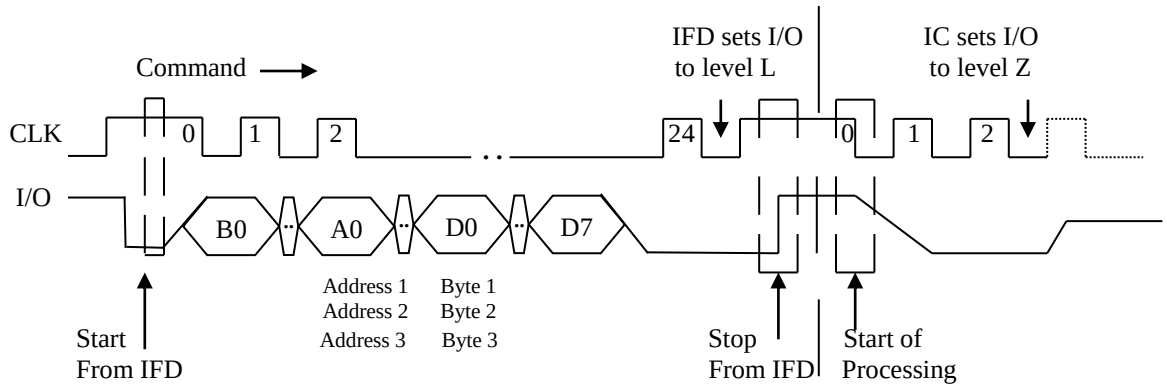


Figure 14: Compare Verification Data

Usage of the Compare Command

The following procedure has to be carried out exactly as described. Any variation results in a failure so that a write and erase cannot be accessed. If the procedure cannot successful complete, the error counter can only be written that means one to zero but cannot be erased. First of all, an error counter bit has to be written to zero by an update security memory command. Then successful execution three-compare verification data command from byte 1 to byte 3 makes erase the error counter possible. Now write and erase access to all memory areas is possible as long as the operation voltage is applied. If error takes place, whole procedure can be repeated with available erased counter bit. Having been enabled, the reference data can be updated like any other information in the main memory.
As transported, the PSC is coded individual agreement with the customer. Thus, knowing the code is indispensable to alter data.

Command	***Control***	***Address***	***Data***	***Remark***
	B7…B0	A7…A0	D7…D0	
Read Security Memory	31_H	No Effect	No Effect	Check Error Counter
Update Security Memory	39_H	00_H	Input Data	Write Free Bit in Error Counter Input Data 0000 0ddd Binary
Compare Verification Data	33_H	01_H	Input Data	Reference Data Byte 1
Compare Verification Data	33_H	02_H	Input Data	Reference Data Byte 2
Compare Verification Data	33_H	03_H	Input Data	Reference Data Byte 3
Update Security Memory	39_H	00_H	FF_H	Erase Error Counter
Read Security Memory	31_H	No Effect	No Effect	Check Error Counter

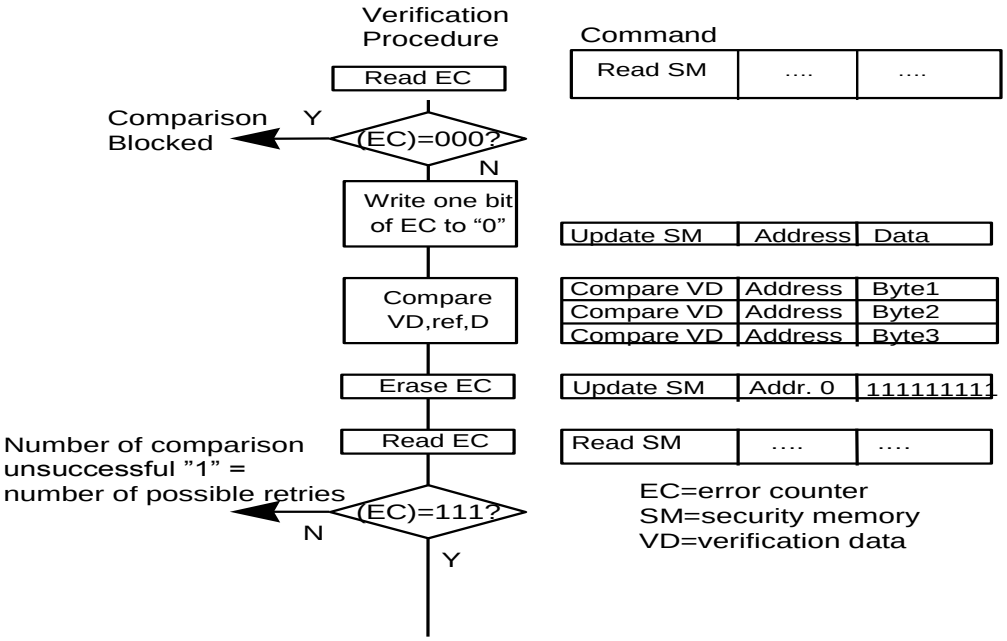


Figure 15: Verification Procedure

Reset Mode

Reset and Answer-To-Reset

Power on Reset

After power on, I/O is high level. A read operation or an Answer-To-Reset must be carried out before any data can be altered.

Break

If RST is set to high level while CLK is low level, any operation is aborted and I/O is switched to high level. To trigger a defined valid reset the necessary minimum duration is t_{RES}=5us.After break, the IC is ready for further operations.

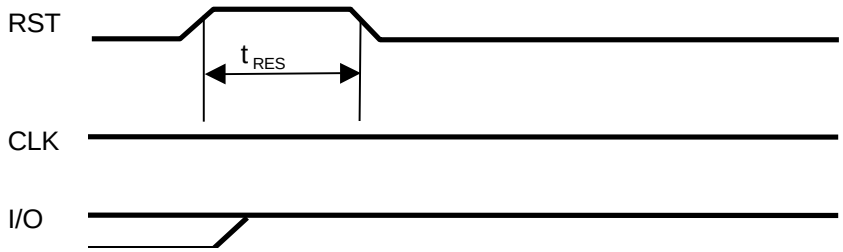


Figure 16: Break

Failures

Behavior of failures:

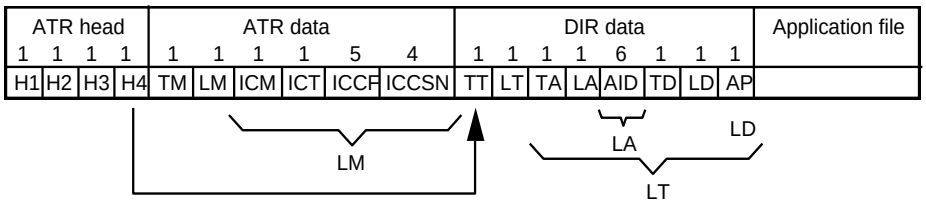
In case of one of the following failures, the chip sets the I/O to high level after 8 clock pulses at the latest.

Possible failures:

- Comparison unsuccessful
- Wrong number of command clock pulse
- Write /erase access to already protected bytes
- Rewrite and erase a protection bit

Coding of the Chip

For security purpose, every chip is irreversibly coded by a scheme. By this way fraud and misuse is excluded. As an example, Figure 17 and Figure 18 show ATR and Directory Data of Structure 1. When transported, ATR header, ICM and ICT are programmed. My-MS programs the IC manufacturer identifier (ICM), IC type (ICT)… My-MS can also program other code depending on the agreement with the customer.



AID	Application identifier	ICCF	Card fabricator id.	LM	Length of manufacter data
AP	Appl. personalizer identifier	ICCSN	Card serial number	LT	Length of application template
ATR	Answer-to-Reset	ICM	IC manufacturer	TA	Tag of AZD
DIR	Directory	ICT	IC type	TD	Tag of discretionary data
H1,H2	Protocol bytes	LA	Length of AID	TM	Tag of manufacter data
H3,H4	ATR historical bytes	LD	Length of data	TT	Tag of application data

Figure 17: Synchronous Transmission ATR and Directory Data

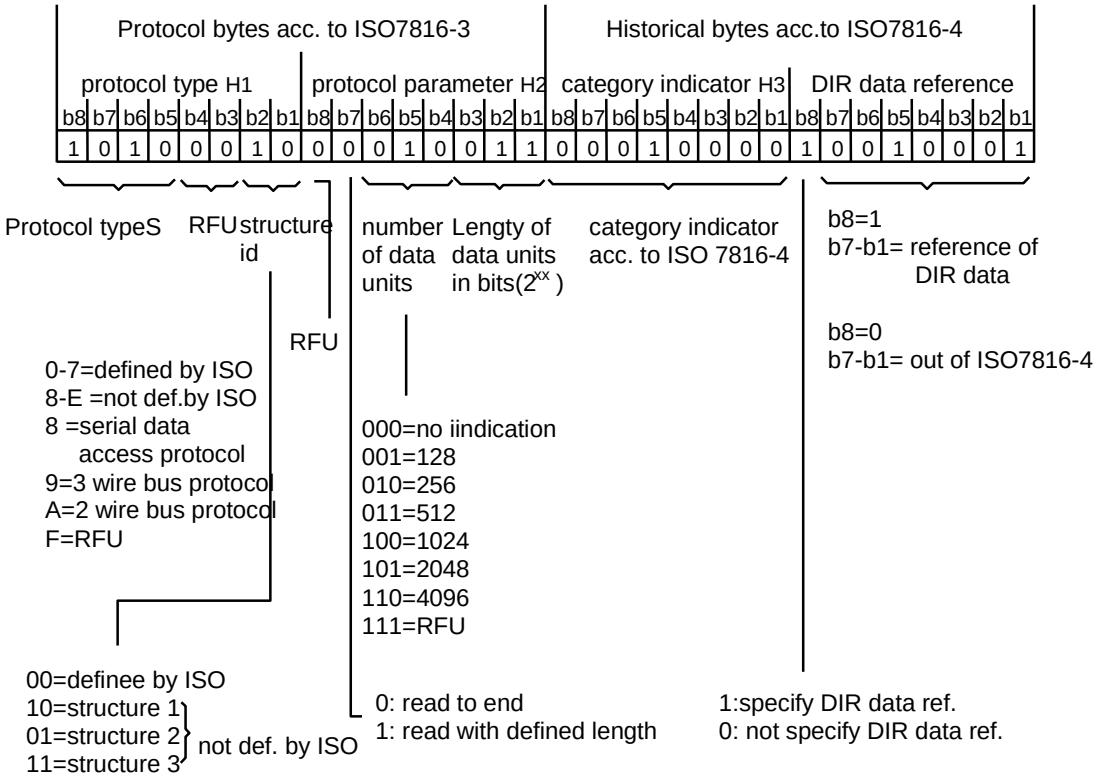


Figure 18: Output Mode

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol		Limits		Unit
		min.	typ.	max	
Supply voltage	V_{CC}	-0.3	-	6	V
Input voltage	V_1	-0.3	-	6	V
Storage temperature	T_{STG}	-40	-	125	°C
Power dissipation	T_{TOT}	0	-	70	mW
Temperature	T_a	0	-	70	°C

DC Characteristics

Parameter	Symbol		Limits		Unit
		min	typ.	max	
Supply					
Supply voltage	V_{CC}	4.5	5	5.5	V
Supply current	I_{CC}	-	3	10	mA
Data input					
H input voltage(I/O,CLK,RST,SELECT)	V_H	V_{CC}-1	-	V_{CC}+0.3	V
L input voltage(I/O,CLK,RST,SELECT)	V_L	V_{GND}-0.2	-	V_{GND}+0.8	V
H inputcurrent (I/O,CLK,RST)	I_H	-	-	50	μA
Data output(I/O)					
L output current	I_L	1	-	-	mA
H current leakage	I_H	-	-	50	μA
Capacitance					
Input capacitance	C_I	-	-	10	pF

AC Characteristics

Parameter	Symbol	Limits		Unit
		min	max	
Clock frequency	CLK	7	50	kHz
Clock high period	t_H	9		μs
Clock low period	t_L	9		μs
Rise time	t_R		1	μs
Full time	t_F		1	μs
Start condition hold time	t_{d1}	4		μs
Delay time	t_{d2}		2.5	μs
Stop condition ,setup time	t_{d3}	4		μs
Data hold time	t_{d5}	1		μs
Data setup time	t_{d7}	1		μs
Start condition, setup time	t_{d8}	4		μs
Reset	t_{RES}	5		μs
Delay time	T_{d9}	2.5		μs
Erase time	t_{ER}	2.5*		ms
Write time	T_{wr}	2.5*		ms
Interval before new start condition	t_{buf}	10		μs

*f=50kHz

ORDERING INFORMATION

Temperature Range: 0º to +70ºC

Order Part Number	Package
MM23SC 4452 - SW	Sorted wafer (standard wafer)
MM23SC 4452 - SN	Sawn wafer (on a ring after backgrinding to 7 mil or specified)
MM23SC 4452 - DW	Die in waffle pack (after backgrinding and saw)
MM23SC 4452 - M2	On a module M2 - 8 pins
MM23SC 4452 - M3	On a module M3 - 6 pins

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