MM60SC6416E

ROM Security Microcontroller Smart Card Chip with EEPROM data memory

21st July 2013

Short Introduction
Revision 1.0

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1.0 INTRODUCTION TO MM60SC6416E

MM60SC6416E is an 8-bit microcontroller smart card IC in 0.18um CMOS technology. The CPU is clocked at maximum of 33Mhz as an option to speed up the processing time. MM60SC6416E features significantly higher performance, high memory capacity and extremely low power consumption. Sleep mode is also available for low power applications.

MM60SC6416E provides 64KBytes read-only ROM and 16KBytes read/write EEPROM with internal 256 Bytes Scratchpad internal RAM (IRAM). A Memory of 2K Bytes External RAM (XRAM) systems provides memory space for fast read/write access.

Communication protocol is according to IS07816-3 with UART modules to simplify IO management and an ETU counter for ETU management. The 32-bit RNG co-processor provided in MM60SC6416E ensures secured random number generation.

MM60SC6416E is also equipped with data scrambling, sensors, clock de-synchronization option and memory encryption to provide highest security chip level.

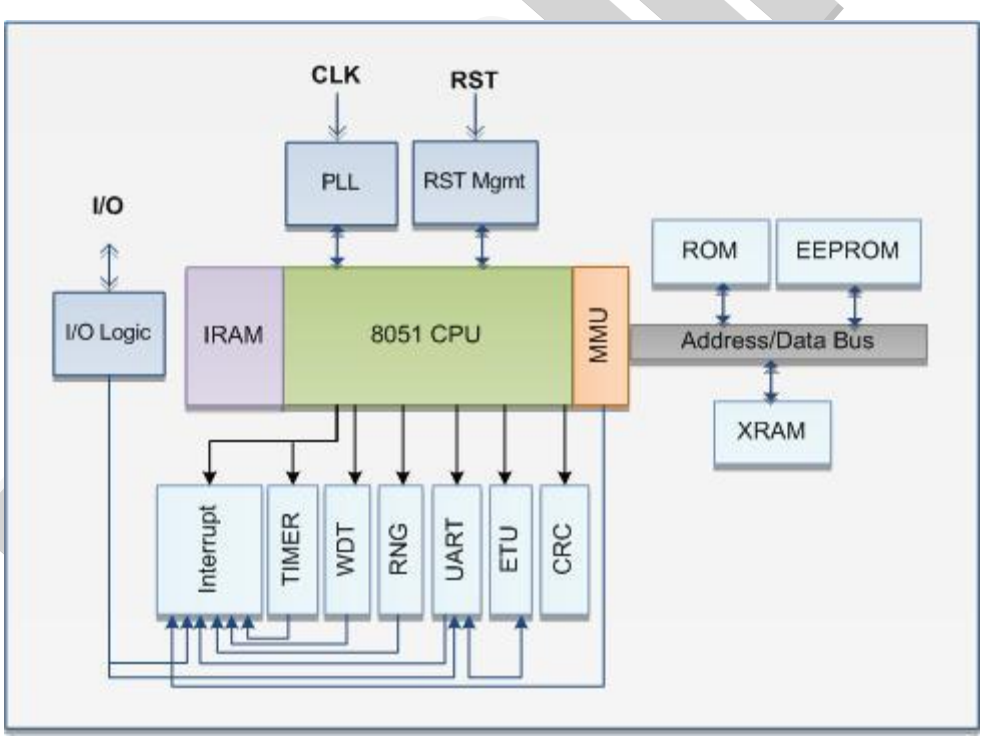

Figure 1-1 Block Diagram of MM60SC6416E

1.1 FEATURES OF THE MM60SC6416E

1.1.1 General

- 0.18µm EEPROM technology.
- 8051 Microcontroller
- ISO7816 pin configuration
- Operating voltage of 2.7V-5.5V.
- Operating temperature -20^{0}C to 80^{0}C
- ESD protection > 4kV (HBM)
- External clock frequency of 1 MHz to 5 MHz
- Maximum internal clock frequency of 33Mhz
- Current consumption < 10mA at 5 MHz.

1.1.2 Security

- Byte-wise data address scrambling.
- Data memory encryption
- Clock de-synchronization option to vary power consumption
- Voltage, temperature and frequency sensor detection for anti-hacking
- Internal power on reset
- Power Supply Low Voltage Detector
- Unique chip identification for each chip

1.1.3 Peripherals

- UART ISO7816 with maximum of 115.2kbps, T=0 and T=1 support.
- Two 16-bit timers and Watchdog Timer
- 32-bit Hardware Random Number Generator.
- Cyclic Redundancy Check (CRC) according to CCIT-16
- Memory Management Unit, MMU
- Elementary Time Unit, ETU Counter
- Interrupt module for peripherals and IO interface

1.1.4 Memory

- Up to 64K Bytes ROM for program memory
- 16K Bytes EEPROM for data memory
  - 64-byte page size
  - Data retention 10 years
  - 500,000 write/erase cycles
- 2K Bytes of XRAM
- CPU Internal data memory of 256 Bytes IRAM.

1.2 PIN DESCRIPTION

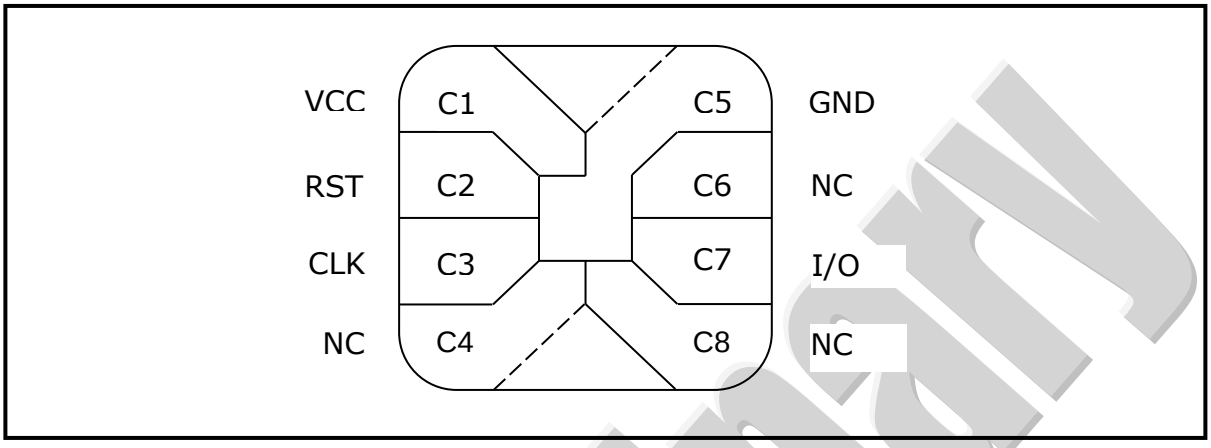

Figure 1-1 Pin Configuration

Table 1-1 Pin Name

Card Contact	Type	Pin Name
C1	VCC	Power
C2	RST	Reset
C3	CLK	Clock Input
C4	NC	No Connection
C5	GND	Ground
C6	NC	No Connection
C7	I/O	Input/Output Connection
C8	NC	No Connection

2.0 ARCHITECTURAL OVERVIEW

The MM60SC6416E is based on the standard 8051. Enhanced features of 8052 are also included with improved speed and power consumption characteristics. It has the same instruction set as in the 8051 family. The MM60SC6416E executes all the standard 8051 instructions approximately 1.5 to 3 times faster in terms of number of clock cycles comparing to the traditional 8051 microcontroller.

3.0 MEMORY ORGANIZATION

The MM60SC6416E has internal and external memories. The internal memories are the Scratchpad RAM and SFR block. The external memories consist of 2Kbytes XRAM, upto 64k bytes ROM, 16k bytes EEPROM and 128 bytes of security memory. The ROM (Program Memory) is used to store instruction op-codes, while the EEPROM (Data Memory) is used to store data.

Figure 4-1 shows the block diagram with internal and external memory.

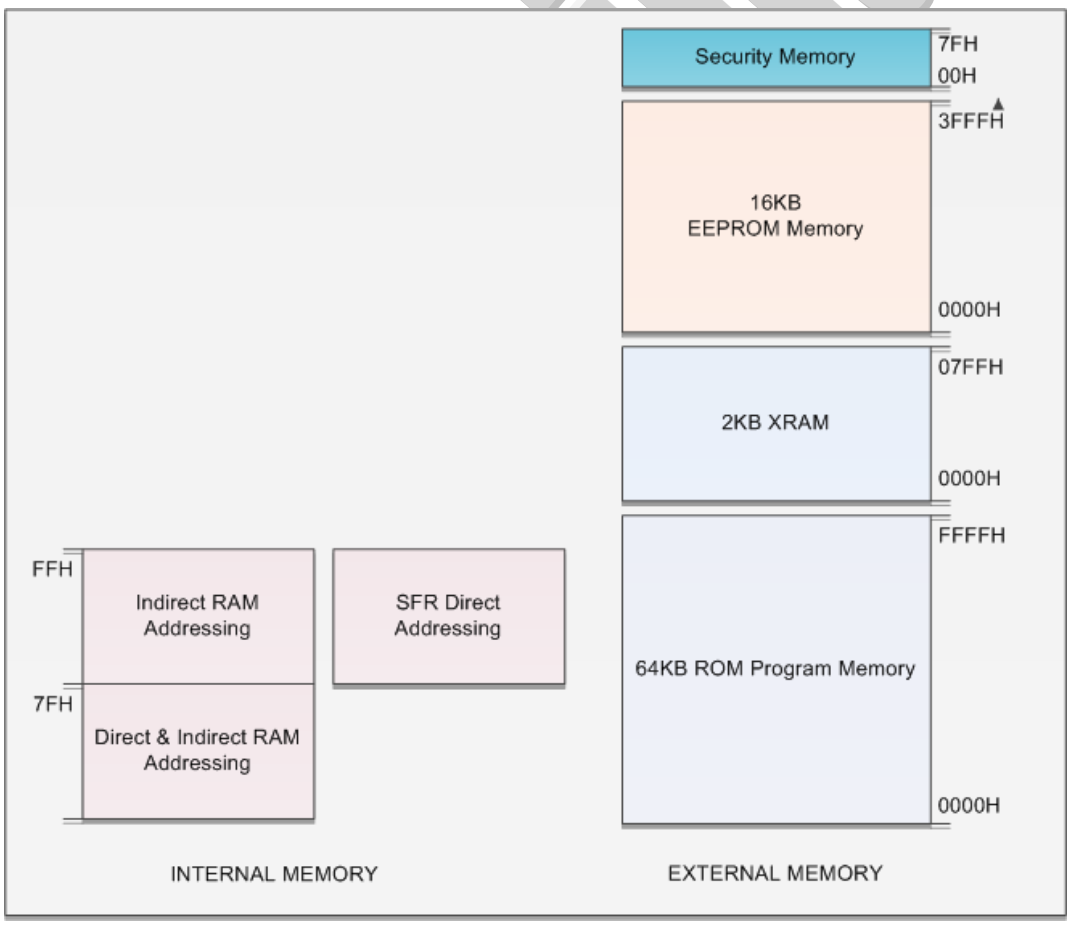

Figure 3-1 Block Diagram with Internal and External Memory

4.0 32-BIT RANDOM NUMBER GENERATOR (RNG)

The MM60SC6416E has Random Number Generator (RNG) that gives output of 32 bits random number on each warm or cold reset or whenever seed generation instruction is issued. Random numbers are used in the authentication of the smart card and the terminal.

5.0 ELEMENTARY TIME UNIT (ETU) COUNTER

ETU counter serves as a timer, for data transfer between reader and the CPU; counts the ETU while the code is running.

The ETU counter is used in an operation that requires a long delay between the APDU and the SW bytes. A wait/null byte is sent out to the reader after APDU bytes. As defined in ISO7816-3, the null byte shall acknowledge the reader that the process is still in progress so that the reader will not send a timeout error. The delay between the leading edges of two consecutive characters sent by the card is configurable.

6.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART) 7816

The MM60SC6416E UART-7816 simplifies IO management to follow ISO7816-3 protocol. It has a baud rate generator that provides the receiver clock and transmitter clock according to the setting on conversion factors, F and adjustment factor, D.

There is also an option to turn off the UART-7816. The UART-7816 also supports T0 and T1 communication protocol. Each FIFO (receiver or transmitter) can be directly accessed by 8051 interfaces. The FIFO receiver and transmitter are asynchronous modules that control the read and write operations.

7.0 CRC COPROCESSOR

The MM60SC6416E has a Cyclic Redundancy Code (CRC) co processor that will generate a 16-bit checksum when using ISO3309 ($x^{16}+x^{12}+x^5+1$). The MM60SC6416E supports two modes of CRC, which are CCITT V.41 and HDLC X25.

The CRC control register, CRCC has a reset bit 0 LRES to reset CRC module, and mode bit 1 LSET to choose CCITT V.41 or HDLC X25. The CRC data register; CRCD will be initialized to 0000h and is read out direct (non-inverted) if mode is CCITT V.41. It will be initialized to 0FFFFh and is read out inverted if mode is HDLC X25.

8.0 ORDERING INFORMATION

Order Part Number	Package
MM60SC6416E – SW	Sorted Wafer
MM60SC6416E – DW	Dice in waffle pack after back grinding to 8 mil.
MM60SC6416E – SR	Sorted wafers on a ring
MM60SC6416E – TR	Modules in tape and reel

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